



Serial - Protocol - SLS

Low-level documentation
needed for implementation
of own host software.

(based on Firmware V1.514, released 05.May 2020)

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1. Structure of the protocol

Byte 0	Byte 1	Byte 2	Byte 3 .. (A-1)	Byte A
S	A	T	D	CRC

- Byte 0: The first byte (S) in a communication frame is implemented as a sync byte. Here comes the sign '!' for an initial communication from the host to the SLS. The returning packet, on the other hand, contains the sync character '?'.
- Byte 1: This byte (A) serves as a counter. The bytes of (Byte 0 .. Byte (A-1)) are counted. **The actual value of the counter may increase with a later firmware version! Therefore we recommend to set the counter from the beginning as a variable in the host software!** (Of course, new firmware version remains backwards compatible, as described in detail below.)
- Byte 2: This byte (T) represents the actual **command / tag** to be processed by the SLS. For details see below. Returned packets return this byte unchanged.
- Byte 3..(A-1): Optional data or parameters for the command to be executed or result data in the response telegram.
- Byte A: After the data bytes, a checksum (CRC) is added, which consists of the sum of all bytes (excluding the checksum itself).

Leading and return packets have the same structure as described above.

2. Status-query:

Status request:

Host sends to SLS:

Byte 0	Byte 1	Byte 2	Byte 3
!	3 _d	'S'	CRC

ACK: Status feedback:

SLS sends to Host:

Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
?	65 _d	'S'	TP	UZK_L	UZK_H	IQ_L	IQ_H

Byte 8	Byte 9	Byte 10	Byte 11	Byte 12	Byte 13	Byte 14	Byte 15
RPM_L	RPM_H	T_F	U_F	C_F	--	--	--

Byte 16	Byte 17	Byte 18	Byte 19	Byte 20	Byte 21	Byte 22	Byte 23
Tmax_DR	Umin_DR	Umax_DR	AMPS_H	AMPS_L	MaxRPM_H	MaxRPM_L	--

Byte 24	Byte 25	Byte 26	Byte 27	Byte 28	Byte 29	Byte 30	Byte 31
--	--	Signal_L	Signal_H	RPM_Limit_L	RPM_Limit_H	MtrCur_Limit_L	MtrCur_Limit_H

Byte 32	Byte 33	Byte 34	Byte 35	Byte 36	Byte 37	Byte 38	Byte 39
RegCur_Limit_L	RegCur_Limit_L	--	--	--	--	--	--

Byte 40	Byte 41	Byte 42	Byte 43	Byte 44	Byte 45	Byte 46	Byte 47
--	--	ID_L	ID_H	--	--	--	--

Byte 48	Byte 49	Byte 50	Byte 51	Byte 52	Byte 53	Byte 54	Byte 55
--	--	--	--	--	--	--	--

Byte 56	Byte 57	Byte 58	Byte 59	Byte 60	Byte 61	Byte 62	Byte 63
--	--	--	--	TE	--	--	--

Byte 64	Byte 65
--	CRC

TP (Powermoduletemperature): Conversion to °C:

$$T = -178,4 + (249 * \sqrt{\frac{854}{598 - TP} - 1})$$

($0 \leq TP \leq 255$ is displayed on $-15,5^\circ\text{C} \leq T \leq +125,4^\circ\text{C}$)

TE (Elkotemperature (only by some SLSi)): Conversion to °C: see TP

UZK_L (low-Byte)
UZK_H (high-Byte):

Conversion: $U[\text{V}] = (\text{UZK} * \text{MaxUZK}) / 1023$

with MaxUZK:

24V ECU: 27,78V

42V ECU: 46,67V

60V ECU: 66,11V

(Scaling factor for the voltage in volts)

AMPS_L
AMPS_H :

maximum releasable current in 0.1 A steps

IQ_L
IQ_H:

actual current (IQ)

Conversion: $I[\text{A}_{\text{eff}}] = \text{IQ} * \text{AMPS} / 10 / 4095$

Bit 15 is the sign bit

ID_L
ID_H :

actual current(ID)

Conversion: $I[\text{A}_{\text{eff}}] = \text{ID} * \text{AMPS} / 10 / 4095$

Bit 15 is the sign bit

MtrCur_Limit_L
MtrCur_Limit_H :

in the data set released motor current

Conversion: $I_{\text{Mot}}[\text{A}_{\text{eff}}] = \text{MtrCur_Limit} * \text{AMPS} / 10 / 4095$

Bit 15 is the sign bit

RegCur_Limit_L
RegCur_Limit_H :

in the data set released generator current

Conversion: $I_{\text{Gen}}[\text{A}_{\text{eff}}] = \text{RegCur_Limit} * \text{AMPS} / 10 / 4095$

Bit 15 is the sign bit

Signal_L
Signal_H:

For the μs signal, the uppermost 6 bits must be masked to 0.
The top bit indicates if the signal is valid.

MaxRPM_L
MaxRPM_H : maximum releasable motor speed in U/min

RPM_L
RPM_H: actual speed
 Conversion: $N[U/min] = (RPM * MaxRPM) / 10922$
 Bit 15 is the sign bit (direction)

RPM_Limit_L
RPM_Limit_H : in the data set released speed
 Conversion: $N [U/min] = (RPM_Limit * MaxRPM) / 10922$
 Bit 15 is the sign bit

T_F (overtemperature fault):
 Bit 7-0

R-0	R-0	R-0	U-0	U-0	U-0	U-0	U-0
SO_T	CMT	LMT	--	--	--	--	--

The value in curly brackets can be found in the Windows Monitor under Parameter-> SLS!

Bit 7 **SO_T:** SwitchOff OverTemp (TP > 100°C, TE > 112°C) =>Failsafe (SLS stopped)
 Bit 6 **CMT:** CutOff MaxTemp (TP > 90°C, TE > 106°C)
 Bit 5 **LMT:** Limit MaxTemp(TP > {Temp_Lim}, TE > 90°C)
 Bit 4-0 **unimplemented:** read as '0'

U_F (over- /undervoltage fault):
 Bit 7-0

R-0	R-0	R-0	U-0	R-0	R-0	R-0	U-0
SO_OV	CMV	LMV	--	SO_UV	CUV	LUV	--

The value in curly brackets can be found in the Windows Monitor under Parameter-> SLS!

Bit 7 **SO_OV:** SwitchOff OverVolt (24V ECU: U > 25,66V
 42V ECU: U > 43,11V
 60V ECU: U > 61,07V)
 Bit 6 **CMV:** CutOff MaxVolt (U > {U_Batt_max})
 Bit 5 **LMV:** Limit_MaxVolt (U > {U_Batt_max} - 1V)
 Bit 4 **unimplemented:** read as '0'
 Bit 3 **SO_UV:** SwitchOff UnderVolt (24V ECU: U < 7,98V
 42V ECU: U < 15,51V
 60V ECU: U < 15,51V
 to SN599 at the SLS: U < 22,49V)
 Bit 2 **CUV:** CutOff_MinVolt (U < {U_Batt_Low})
 Bit 1 **LUV:** Limit_MinVolt (U < {U_Batt_Lim})
 Bit 0 **unimplemented:** read as '0'

C_F (Error of the internal control):

Bit 7-0

R-0	U-0	R-0	U-0	R-0	U-0	U-0	R-0
PL_F	--	ZS_F	I_F	OS_F	LL_F	2PH_F	FS

Bit 7 **PL_F**: PhaseLoss_Flt -> stop+retry
 Bit 6 **unimplemented**: read as '0'
 Bit 5 **ZS_F**: ZeroSpd_Flt -> stop+retry
 Bit 4 **I_F**: I_Offset_Flt -> stop+retry
 Bit 3 **OS_F**: OvrSpd_Flt -> stop+retry
 Bit 2 **LL_F**: Loadless_Fault -> stop+retry
 Bit 1 **2PH_F**: 2-Phase-PWM
 Bit 0 **FS**: Failsafe_STOP (SLS stopped) -> check -> clear Error

Tmax_DR (Temp Max derate Register):

Umin_DR (Overvoltage derate Register):

Umax_DR (Undervoltage derate Register): These 3 registers give more detail on how far is down regulated.

Value ranges for the 3 Derate registers:

0x40 (it is not yet regulated) until

0x00 (controller switches off)

NACK: transmission error:

SLS sends to Host:

Byte 0	Byte 1	Byte 2	Byte 3
'?'	3 _d	'?'	CRC

2.1. Servo signal override:

Status request:

Host sends to SLS:

Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
!	7 _d	'S'	1 _d	Active	Signal_L	Signal_H	CRC



To prevent a timeout, the TAG "Servo signal override" must be sent cyclically. The timeout is 300ms.

Active :

0xAA Signal will be overwritten.
0x00 Signal will not be overwritten.

Signal_L
Signal_H :

Signal specification in μs permissible range:
800 .. 2200 μs

ACK: Status feedback:

SLS sends to Host see 2

2.2. Servosignal offset:

Status request:

Host sends to SLS:

Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5
!	5 _d	'S'	2 _d	Servooffset	CRC

Servooffset :

Servo signal offset in μsec
Value range: $\pm 127 \mu\text{sec}$
The sent offset becomes permanent
stored in the controller.

ACK: Status feedback:

SLS sends to Host see 2

2.3. Option Control Panel (chargeable):

Status request:

Host sends to SLS:

Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
'!	14 _d	'S'	3 _d	Active	Control	SPD_WMo n_L	SPD_WMo n_H

Byte 8	Byte 9	Byte 10	Byte 11	Byte 12	Byte 13	Byte 14
MtrCur_W Mon_L	MtrCur_W Mon_H	RegCur_W Mon_L	RegCur_W Mon_H	Accel_WM on	Decel_WM on	CRC



To prevent a timeout, the TAG "Servo signal override" must be sent cyclically. The timeout is 300ms.

Active : 0xAA Signal will be overwritten.
0x00 Signal will not be overwritten.

Control:
Bit 7-0

U-0	U-0	U-0	U-0	U-0	W	W	W
--	--	--	--	--	Direction	Start/Stop	parking brake_ active

Bit 7-3 **unimplemented:** read as '0'
 Bit 2 Direction
 Bit 1 Stop = 0; Start = 1
 Bit 0 parking brake active = 1, the motor is braked by short circuit of the 3 phases.

SPD_WM_L
SPD_WM_H : speed specification, value range: 0 .. 1023
 1023 corresponds to the engine speed released in the parameters
(RPM_Limit)

MtrCur_WMon_L
MtrCur_WMon_H : motor current specification, value range: 0 .. 1023
 1023 corresponds to the motor current released in the parameters
(MtrCur_Limit)

RegCur_WMon_L
RegCur_WMon_H : generator current specification, value range: 0 .. 1023
 1023 corresponds to the motor current released in the parameters
(RegCur_Limit)

Accel_WMon: acceleration rate, value range: 1 .. 255
Decel_WMon: deceleration rate, value range: 1 .. 255

ACK: Status feedback:

SLS sends to Host see 2

3. Error reset/ SW-Reset

Error reset:

Host sends to SLS:

Byte 0	Byte 1	Byte 2	Byte 3	Byte 4
'!	4 _d	'R'	PAR	CRC

PAR:

Bit 7-0

W-0	U-0	U-0	W-0	U-0	U-0	U-0	U-0
Reboot	0	0	Clear	0	0	0	0

Bit 7 **Reboot:** complete software will be restarted (via reset vector)

Bit 6-5 **unimplemented:** write as '0'

Bit 4 **Clear:** all errors are cleared

Bit 3-0 **unimplemented:** write as '0'

ACK -> acknowledge:

SLS sends to Host:

Byte 0	Byte 1	Byte 2	Byte 3
'?'	3 _d	'R'	CRC

NACK: transmission error:

SLS sends to Host:

Byte 0	Byte 1	Byte 2	Byte 3
'?'	3 _d	'?'	CRC